IN THE CLAIMS:

1. (currently amended) A power transistor comprising

a plurality of vertical PNP transistors formed on a P-type silicon substrate~~, wherein the vertical PNP transistors have an N+ type electrode layer,~~

~~a plurality of electrode portions of~~ an N^+ type buried layer formed to isolate the P-type silicon substrate and the plurality of vertical PNP transistors from each other, and

at least one electrode portion of the N^+ type buried layer, which has an N^+ type diffusion layer contacting the N^+ type buried layer, wherein

the at least one electrode portion is located in an active region of the power transistor surrounded from all around by the vertical PNP transistors

~~an N^+ type diffusion layer sandwiched between at least two of the plurality of vertical PNP transistors as well as under, contacting and surrounding a portion of the N^+ type electrode layer, and extending to contact the N^+ type buried layer~~.

2. (original) The power transistor according to Claim 1, wherein

at least part of the electrode portion is provided under common emitter metal lines of the power transistor routed on the active region of the power transistor.

3. (currently amended) The power transistor according to Claim 1, wherein

the at least one electrode portion is ~~portions are~~ provided on the N^+ type buried layer and formed of an N^+ type electrode layer for making ohmic contact and an N^+ type diffusion layer.

4. (original) The power transistor according to Claim 3, wherein

the N^+ type diffusion layer is formed simultaneously with an N^+ type base well layer as a base region of the plurality of vertical PNP transistors.

5. (original) The power transistor according to Claim 3, wherein

the N^+ type diffusion layer is formed at a range of dopant level of 1×10^{16} to 1×10^{17} atoms/cm^3, which is heavier than that of an N-type epitaxial layer formed on the P-type silicon substrate.

6. (original) The power transistor according to Claim 3, wherein

the N^+ type diffusion layer is formed so that dopants are diffused until they reach the N^+ type buried layer present on a bottom face of the power transistor.

7. (currently amended) The power transistor according to Claim 1, wherein

the at least one electrode portion is ~~singularity or plurality of electrode portions are~~ placed so as to be uniformly spaced from ~~their~~ respectively adjacent electrode portions.

8. (original) A semiconductor integrated circuit characterized by using the power transistor as defined in Claim 1.

9. (previously presented) A power transistor having suppression of problematic leak current, the power transistor comprising:

a plurality of vertical PNP transistors formed on a P-type substrate, each PNP transistor having a P^+ type collector, an N+ type base well formed at a base region, a P^+ type emitter layer and an N^+ type base layer;

P^+ type collector buried layers formed under the N^+ type base well;

an N^+ type buried layer isolating the P-type substrate from the P^+ type collector;

an N-type epitaxial layer formed over a surface of the P-type substrate;

an N^+ type electrode layer; and

a plurality of N^+ type diffusion layers formed at electrode portions within an active region under, contacting and surrounding the N^+ type electrode layer to reduce resistance of the N-type epitaxial layer by extending therethrough to contact the N^+ type buried layer, wherein at least one of the N^+ type diffusion layers passes between the P^+ type collector buried layers.